CLAIMS

WHAT IS CLAIMED:

1. A built-in self-test controller, comprising:

a first frequency domain in which logic built-in self-test operations are performed;

a second frequency domain in which memory built-in self-test operations are performed; and

a third frequency domain in which a test interface operates.

2. The built-in self-test controller of claim 1, wherein a clock signal for the first frequency domain is derived from a clock frequency for the third frequency domain.

3. The built-in self-test controller of claim 2, wherein a clock signal for the second frequency domain is derived from the clock signal for the first frequency domain.

4. The built-in self-test controller of claim 1, wherein:

the first frequency domain operates at a 150 MHz frequency;

the second frequency domain operates at a 75 MHz frequency; and

the third frequency domain operates at a 10 MHz frequency.

5. The built-in self-test controller of claim 1, wherein the first frequency domain generates at least one of:

a plurality of level sensitive scan device clock signals; and

a plurality of step clock signals.

6. The built-in self-test controller of claim 1, wherein the first frequency domain generates a plurality of step clock signals.

7. The built-in self-test controller of claim 1, wherein the first frequency domain, includes:

a logic built-in self-test engine capable of executing a logic built-in self-test and storing the results thereof; and

a multiple input signature register capable of storing the results of an executed logic built-in self-test.

8. The built-in self-test controller of claim 7, wherein the logic built-in self-test engine comprises:

a logic built-in self-test state machine; and

a pattern generator.

9. The built-in self-test controller of claim 1, wherein the second frequency domain includes a memory built-in self-test engine capable of executing a memory built-in self-test.

10. The built-in self-test controller of claim 9, wherein the second frequency domain further comprises a memory built-in self-test signature register capable of storing the results of the memory built-in self-test.

11. The built-in self-test controller of claim 9, wherein the memory built-in self-test engine comprises:

a memory built-in self-test state machine; and

a nested memory built-in self-test engine operating the memory built-in self-test state machine.

12. The built-in self-test controller of claim 9, wherein the memory built-in self-test engine comprises:

a plurality of alternative memory built-in self-test state machines; and

a nested memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines.

13. An integrated circuit device, comprising:

a plurality of memory components;

a logic core;

a testing interface; and

a built-in self-test controller, including:

a first frequency domain in which logic built-in self-test operations are performed;

a second frequency domain in which memory built-in self-test operations are performed; and

a third frequency domain in which a test interface operates.

14. The built-in self-test controller of claim 13, wherein a clock signal for the first frequency domain is derived from a clock frequency for the third frequency domain.

15. The built-in self-test controller of claim 13, wherein:
the first frequency domain operates at a 150 MHz frequency;
the second frequency domain operates at a 75 MHz frequency; and
the third frequency domain operates at a 10 MHz frequency.

16. The built-in self-test controller of claim 13, wherein the first frequency domain generates a plurality of level sensitive scan device clock signals.

17. The built-in self-test controller of claim 13, wherein the first frequency domain generates a plurality of step clock signals.

18. The built-in self-test controller of claim 13, wherein the first frequency domain, includes:
a logic built-in self-test engine capable of executing a logic built-in self-test and storing the results thereof; and
a multiple input signature register capable of storing the results of an executed logic built-in self-test.

19. The built-in self-test controller of claim 13, wherein the second frequency domain includes a memory built-in self-test engine capable of executing a memory built-in self-test.

20. The integrated circuit device of claim 13, wherein the memory components include a static random access memory device.

21. The integrated circuit device of claim 13, wherein testing interface comprises a Joint Test Action Group tap controller.

22. A method for use in performing a built-in self-test, the method comprising:
receiving an external clock signal in a testing interface, the external clock signal defining a first frequency domain;
generating a first internal clock signal, the first internal clock signal defining a second frequency domain in which a logic built-in self-test may be performed; and

generating a second internal clock signal, the second internal clock signal defining a third frequency domain in which memory built-in self-test may be performed.

23. The method of claim 22, wherein generating the first internal clock signal includes generating the first internal clock signal from the external clock signal.

24. The method of claim 23, wherein generating the second internal clock signal includes generating the second internal clock signal from the first internal clock signal.

25. The method of claim 22, wherein the external clock signal has a frequency of 75 MHz, the first internal clock signal has a frequency of 150 MHz, and the second internal clock signal has a frequency of 75 MHz.

26. The method of claim 22, further comprising at least one of:

generating a plurality of level sensitive scan device clock signals in the second frequency domain; and

generating a plurality of step clock signals.

27. The method of claim 22, further comprising:

performing a logic built-in self-test from the second frequency domain; and

storing the results of the executed logic built-in self-test.

28. The method of claim 27, wherein storing the results of the executed logic built-in self-test includes storing the results in a multiple input signature register.

29. The method of claim 22, further comprising performing a memory built-in self-test from the third frequency domain.

30. The method of claim 29, wherein the memory built-in self-test includes:

resetting a memory built-in self-test engine;

initiating a plurality of components and signals in the third frequency domain upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

flushing the contents of a plurality of memory components to a known state after initialization of the components and the signals; and

testing the flushed memory components.

31. A method for testing an integrated circuit device, the method comprising:

interfacing the integrated circuit device with a tester;

performing a built-in self-test, including:

receiving an external clock signal in a testing interface from the tester, the external clock signal defining a first frequency domain;

generating a first internal clock signal, the first internal clock signal defining a second frequency domain in which a logic built-in self-test may be performed; and

generating a second internal clock signal, the second internal clock signal defining a third frequency domain in which memory built-in self-test may be performed; and

obtaining the results of the built-in self-test.

32. The method of claim 31, wherein generating the first internal clock signal includes generating the first internal clock signal from the external clock signal.

33. The method of claim 31, wherein the external clock signal has a frequency of 75 MHz, the first internal clock signal has a frequency of 150 MHz, and the second internal clock signal has a frequency of 75 MHz.

34. The method of claim 31, wherein performing the built-in self-test includes performing a logic built-in self-test.

35. The method of claim 31, further comprising:

performing a logic built-in self-test from the second frequency domain; and

storing the results of the executed logic built-in self-test.